

Analytical calculation of resonant inductance for zero voltage switching in phase-shifted full-bridge converters

Article

Accepted Version

Hallworth, M., Potter, B. and Shirsavar, A. (2013) Analytical calculation of resonant inductance for zero voltage switching in phase-shifted full-bridge converters. *Power Electronics, IET*, 6 (3). pp. 523-534. ISSN 1755-4543 doi: <https://doi.org/10.1049/iet-pel.2012.0461> Available at <https://centaur.reading.ac.uk/31750/>

It is advisable to refer to the publisher's version if you intend to cite from the work. See [Guidance on citing](#).

To link to this article DOI: <http://dx.doi.org/10.1049/iet-pel.2012.0461>

Publisher: IET

All outputs in CentAUR are protected by Intellectual Property Rights law, including copyright law. Copyright and IPR is retained by the creators or other copyright holders. Terms and conditions for use of this material are defined in the [End User Agreement](#).

www.reading.ac.uk/centaur

CentAUR

Central Archive at the University of Reading

Reading's research outputs online

Analytical Calculation of Resonant Inductance for Zero Voltage Switching in Phase-Shifted Full-Bridge Converters

Michael Hallworth, *Member, IEEE*, B. A. Potter, *Member, IEEE*, and Seyed Ali Shirsavar.

Abstract

The phase shift full bridge (PSFB) converter allows high efficiency power conversion at high frequencies through zero voltage switching (ZVS); the parasitic drain-to-source capacitance of the MOSFET is discharged by a resonant inductance before the switch is gated resulting in near zero turn-on switching losses. Typically, an extra inductance is added to the leakage inductance of a transformer to form the resonant inductance necessary to charge and discharge the parasitic capacitances of the PSFB converter. However, many PSFB models do not consider the effects of the magnetizing inductance or dead-time in selecting the resonant inductance required to achieve ZVS. The choice of resonant inductance is crucial to the ZVS operation of the PSFB converter. Incorrectly sized resonant inductance will not achieve ZVS or will limit the load regulation ability of the converter. This paper presents a unique and accurate equation for calculating the resonant inductance required to achieve ZVS over a wide load range incorporating the effects of the magnetizing inductance and dead-time. The derived equations are validated against PSPICE simulations of a PSFB converter and extensive hardware experimentations.

Index Terms

DC-DC power conversion, quasi-resonant converter, phase shift full bridge, zero voltage switching.

The authors are with the School of Systems Engineering, The University of Reading, England. Corresponding author: Michael Hallworth. E-mail: m.a.hallworth@pgr.reading.ac.uk. The paper in its current form has been submitted solely to the IET Power Electronics journal and has not been presented at a conference.

I. INTRODUCTION

High frequency power conversion allows the use of smaller magnetic components resulting in a real-estate advantage. However, an increase in frequency also increases the switching losses and thus limits the efficiency of the power converter. Switch-on losses result from the energy stored in the output capacitance of a MOSFET, from drain-to-source, being discharged as the MOSFET is turned on. The energy dissipation during this hard switching event is proportional the square of the voltage across the MOSFET [1], [2]. Soft switching of the MOSFET, in the form of ZVS, can be used to turn the switch on with zero voltage across the drain-to-source junction and thus near zero turn-on losses. Soft switching in this manner eliminates turn-on switching losses and increases the overall efficiency of converters [3], [4], [5]. Soft switching with IGBTs can also be achieved [6], however, for the topology discussed in this paper the analysis is performed using MOSFET switches. Furthermore, it may be preferable to use zero current switching at zero crossing with IGBTs rather than ZVS [7].

Resonant converters offer one method of achieving soft switching. However, in order to achieve load regulation the switching frequency of the converter is varied around the frequency of its resonant tank [8]; this presents some disadvantages. The conduction losses within resonant converters can be significant [9] and the frequency is modulated over a large range which is not ideal for the design of magnetic components [9], [10].

The advantages of soft switching can be applied to conventional PWM converters by combining the PWM switch with a resonant tank [2] to create a quasi-resonant converter (QRC). Constant frequency of operation, a desirable attribute of PWM converters, can then be used with soft switching converters through a phase shift control technique. The phase-shift full-bridge (PSFB) converter is an example of a soft switching converter topology which provides high frequency and high efficiency conversion [1], [10].

In order to achieve soft switching in a PSFB converter an additional inductance is typically added to the primary current path to form the resonant inductance. This resonant inductance is often partly formed by the leakage inductance of the transformer present in the PSFB converter topology. The leakage inductance of the transformer does not necessarily need to be minimized as a larger resonant inductance allows ZVS over a greater load range. Additional leakage inductance can even be added to the transformer in order to increase the size of the resonant inductance [11]. During the transition intervals the energy stored in the resonant inductance is used to charge and discharge the parasitic capacitances of the MOSFET in a quasi-sinusoidal manner resulting in near zero voltage across the drain-to-source terminals of the MOSFET switches. In practice, as the intrinsic diode of the MOSFET will now be conducting, there will be a negative forward diode drop across the drain-to-source terminals. However, generally this is small in comparison to the supply voltage. Following this transition interval, the switches can be turned on with near zero turn-on losses.

The resonant inductance limits the maximum voltage gain of the converter as the current must commute during each switching cycle. The result is an effective duty applied to the secondary side output filter that is less than the primary side duty [12]. An unnecessarily large resonant inductance would achieve ZVS but would also result in longer transition times and reduce the maximum voltage gain of the converter by increasing the period referred to

as the lost duty period, ΔD . Conversely, a resonant inductance that is too small would not fully charge or discharge the parasitic drain-to-source capacitances and thus ZVS would not be achieved. Previous analyses [13], [14], [15], [16] do not include the effects of the dead-time between switching with respect to achieving ZVS. This paper explains why this factor is important and how ZVS can be lost if the correct resonant inductance is not selected for a specified dead-time.

An investigation by Sabate et al. [13] determined that the resonant inductance should store equal energy to that stored in the parasitic capacitances that need to be charged or discharged within the system. The energy required for this resonant transition depends upon the total capacitance which is a combination of MOSFET output capacitance and any transformer winding capacitances. However, this method may result in an insufficient value of resonant inductance as ZVS will not be achieved if the resonant inductor current reaches zero before the final switch is turned on at the end of the dead-time. This will occur when the dead-time is greater than the resonant transition time; as is the case for most converters.

Furthermore, a critical current has been identified [13] below which ZVS is lost for a specific resonant inductance. This analysis has provided some insight into the point at which the converter will re-enter hard switching. However, to date there have been no precise methods of selecting a resonant inductance in order to guarantee ZVS for a specified minimum load. Therefore at low loads ZVS could be lost. The model presented in this paper addresses this issue and the resulting equations allow the designer to achieve ZVS with the widest possible load regulation.

It has been identified that the magnetizing current can also assist in the resonant transition and allow ZVS over a greater load range [14], [17] where normally the resonant inductor current would no longer be sufficient. This additional magnetizing current is beneficial at light loads [15]. An equation is given for the maximum magnetizing inductance possible to achieve ZVS [16]. However, none of the current analyses offer a method for calculating the resonant inductance whilst taking into consideration the magnetizing inductance. The model described in this paper includes the effects of the magnetizing current across the entire load range; this current would be significant in transformers with a low magnetizing inductance. Methods exist to improve the ZVS range of the PSFB converter, by inserting additional reactive or magnetic components [18], [19], [20], [21], [22]. However, these methods have the disadvantage of further complexity. The analysis presented in this paper refers to the standard PSFB converter defined by and credited to Steigerwald [23].

Whilst an increased magnetizing current would assist in both the resonant transitions and achieving ZVS, it would also increase the conduction losses of the converter due to the increased circulating current. Therefore, the magnetizing inductance should be maximized in order to reduce this circulating current. Alternatively, a method of reducing this current such as using a split primary winding [24] or additional switches and switching intervals [25] could be employed. However, both of these methods required additional switches or magnetic components which will increase the physical dimensions of the converter and component cost. Whilst this may be acceptable in some applications, it is important to consider the most efficient mode of operation of the conventional PSFB converter before inserting additional components to increase the ZVS range. The analysis provided in this paper can be applied to variants of the conventional PSFB converter that aim to increase this range further still.

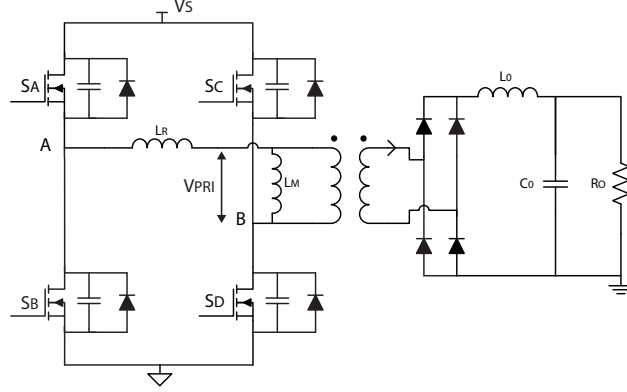


Fig. 1. PSFB converter circuit diagram

Building on the aforementioned work, this paper presents a method for calculating the resonant inductance required to achieve zero voltage switching over a wide load range taking into consideration all of the pertinent design characteristics. This method is verified through a design example. Section II describes the equation for calculating the required resonant inductance for the ZVS load range. In Section III a steady state analysis of the PSFB converter is given in order to derive the terms necessary to calculate the resonant inductance. The analysis presented in Section III incorporates the magnetizing inductance and dead-times into the equations defining the key currents and voltages for each sub-interval of one steady state switching cycle.

The derived equations are verified in Section IV using thorough PSPICE simulations of a PSFB design example and detailed experimental results from a comparative hardware implementation. Oscilloscope plots are also provided. This design example shows that, with a known magnetizing inductance and dead-time, the additional inductance required to achieve ZVS can be calculated accurately.

II. ANALYTICAL CALCULATION OF RESONANT INDUCTANCE

A. PSFB Converter Operation

The PSFB converter, in its original form [23], is shown in Figure 1. Switches S_A and S_B in Figure 1 are driven with complimentary PWM with a dead-time inserted between switching. The same principle applies to switches S_C and S_D .

In Figure 2 the operation of the PSFB converter is shown over half of the switching period. Figure 2a shows the gate drive signals for switches S_B and S_C and the voltage across the drain-source terminal and thus parasitic capacitance of these switches. The voltage across the parasitic capacitance of switch S_C is discharged to zero by the action of the resonant inductance during time period t_4 to t_5 and the switch could be turned on with ZVS after t_5 , however, the dead-time lasts until t_6 . If the resonant inductance were too small the current through the inductance would collapse to zero before the complete resonant charge or discharge of capacitances could occur; ZVS would not be achieved.

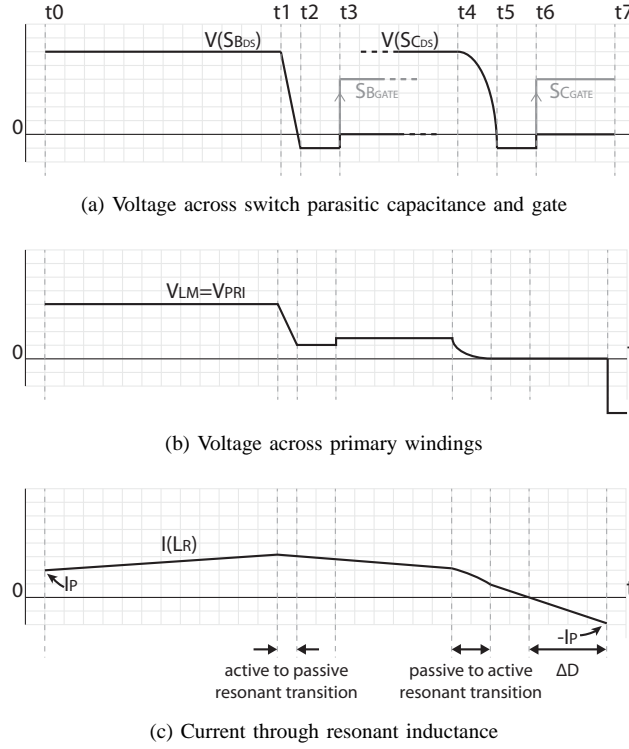


Fig. 2. PSFB converter waveforms during one half of the switching cycle

It is also imperative to consider the length of the dead-time, t_4 to t_6 , in selecting the correct resonant inductance. ZVS will be lost if the ramping current through the resonant inductor reaches zero before the final switch in the sequence is turned on at t_6 , at the end of the dead-time. The diode in anti-parallel with the final switch would become reverse biased and the voltage across the switch would increase to the supply voltage. Thus, the resonant inductance must be sized such that, at minimum load, the current through the resonant inductance reaches zero immediately following the end of the dead-time when the final switch is turned on.

Calculating the resonant inductance to achieve this requirement will inherently minimize the lost duty period, ΔD during t_6 to t_7 , increasing the range for which the converter can regulate, and maintaining ZVS for the minimum load; previously this process has not been achieved analytically. The work presented in this paper gives rise to an equation for calculating the resonant inductance incorporating the length of the dead-time and guaranteeing ZVS across the load range. The current through the resonant inductance when the switch is turned on, at time t_6 , will be zero for the minimum inductance required to achieve ZVS. This requirement provides the premise for calculating the required resonant inductance.

B. Calculating Resonant Inductance for ZVS

Consider the trace representing I_{L_R} during period t_5 to t_6 in Figure 2c. For the minimum inductance required in order to achieve ZVS at t_6 , I_{L_R} must have ramped from the value at t_5 to zero at t_6 . Using the equation for

inductance in (1):

$$L = V \cdot \frac{\Delta t}{\Delta I} \quad (1)$$

The equation for calculating the required resonant inductance is expressed analytically in (2):

$$L_R = V_{L_R}(t_5, t_6) \cdot \frac{t_{5,6}}{0 - I_{L_R}(t_5)} \quad (2)$$

Thus, the resonant inductor size is calculated based on the resonant inductor current, I_{L_R} , ramping to zero from the value of the current at time t_5 . Where $V_{L_R}(t_5, t_6)$ is the voltage across the resonant inductor during the time period t_5 to t_6 and $I_{L_R}(t_5)$ is the current through the resonant inductance at time period t_5 as shown in Figure 2c.

The current through the resonant inductance at time period five, $I_{L_R}(t_5)$, and the voltage across the resonant inductance will be derived through detailed circuit analysis of the PSFB converter provided in Section III of this paper. The analysis of the converter is performed over half of the switching period; the remaining half period is identical but opposite in sign. This half switching period is subdivided into eight intervals, t_0 to t_7 , and a full description of each time interval is provided in Section III.

III. EQUATION DERIVATION

The converter operates at a switching frequency f_s and $T = 1/f_s$. The factor of $T/2$ appears in many of the equations herein as the analysis is performed over one half of the switching period. The remaining half of the switching period is identical but uses the opposite pair of switches. The operation of the PSFB converter is described by a set of equations relating the key currents and voltages. The voltage across the primary windings of the transformer is derived for each subinterval. This will allow the equations necessary for calculating the resonant inductance to be derived.

The following terms are defined:

D	Primary side duty.
D_{EFF}	Effective secondary side duty.
ΔD	Duty cycle loss. $\Delta D = D - D_{EFF}$.
t_{DT}	Required dead time.
$t_{1,2}$	Active-to-passive resonant transition time.
$t_{4,5}$	Passive-to-active resonant transition time.
n	Transformer turns ratio $n = N_S/N_P$. Where N_P and N_S are the number of primary and secondary turns respectively.
V_S	Supply voltage.
V_{OUT}	Output voltage.
I_O	Output current.
L_R	Resonant inductance.
C_R	Total resonant capacitance.

L_M	Transformer magnetizing inductance.
L_0	Inductance of the output filter.
V_{RD}	Diode forward voltage drop due to a rectifying diode.
V_{MD}	Diode forward voltage drop due to a MOSFET intrinsic diode.
$n.V_{PRI}(t)$	Voltage across the secondary windings of the transformer at time t .
I_P	Current through the primary path/resonant inductance at the start of the half switching period. At the end of the half switching period it is the same magnitude but opposite in sign.
I_{MAG}	Current through the magnetizing inductance at the start of the half switching period. At the end of the half switching period it is the same magnitude but opposite in sign.
I_S	Current through the secondary path/output inductor at the start of the half switching period.

The analysis of the converter in this section derives the changes in three key currents as there are three current loops within the PSFB converter circuit:

$I_{L_R}(t)$	Current through resonant inductance and primary current path.
$I_{L_M}(t)$	Current through magnetizing inductance.
$I_{L_0}(t)$	Current through output inductor.

Furthermore, three key voltages are derived in order to determine these key currents:

$V_{L_R}(t)$	Voltage across the resonant inductance.
$V_{L_M}(t)$	Voltage across the magnetizing inductance, and thus primary windings of the transformer $V_{PRI}(t)$.
$V_{L_0}(t)$	Voltage across the output inductor.

These key voltages and currents are solved to find the voltage across the primary winding of the transformer $V_{PRI}(t)$. All steps necessary to repeat the derivation and achieve the same results are given.

A. Operation During $t = t_0$ to t_1

During this period switches S_A and S_D are on (S_B and S_C are off). The supply voltage V_S is applied across the resonant and magnetizing inductance and power is delivered to the load. The reflected output current, plus the magnetizing current, is flowing through the primary current path, $I_{L_R}(t)$. This period lasts for $D_{EFF} \cdot \frac{T}{2}$ and is the power delivery interval. The key changes in current over this time period are defined as:

$$\Delta I_{L_0}(t_0, t_1) = \frac{V_{L_0}(t)}{L_0} \cdot \Delta t \quad (3)$$

$$\Delta I_{L_R}(t_0, t_1) = \frac{V_{L_R}(t)}{L_R} \cdot \Delta t \quad (4)$$

$$\Delta I_{L_M}(t_0, t_1) = \frac{V_{L_M}(t)}{L_M} \cdot \Delta t \quad (5)$$

Where Δt is the duration of the time interval. During this time interval, $V_{L_0}(t)$, $V_{L_R}(t)$ and $V_{L_M}(t)$ are effectively constant. Therefore the rate of change of current will also be constant as the supply voltage V_S is clamped across

the resonant and magnetizing inductance. The relationship between the changes in current over each time period is derived using the reflected output current, the current through the resonant inductance, the current through the magnetizing inductance and Kirchhoff's current law at the beginning and end of each time period. This relationship is given in (6).

$$\Delta I_{L_0}(t) \cdot n = \Delta I_{L_R}(t) - \Delta I_{L_M}(t) \quad (6)$$

The key voltages (7) to (9) are derived by analyzing the voltages around the closed loops of the PSFB converter during this time period. These are substituted into Equations (3) to (5) in order to find the change in inductor currents over this time period.

$$V_{L_0}(t_0, t_1) = n \cdot V_{PRI}(t) - 2 \cdot V_{RD} - V_{OUT} \quad (7)$$

$$V_{L_R}(t_0, t_1) = V_S - V_{PRI}(t_0, t_1) \quad (8)$$

$$V_{L_M}(t_0, t_1) = V_{PRI}(t_0, t_1) \quad (9)$$

Finally, (3) to (5) are substituted into (6) in order to derive an equation for the voltage across the primary winding of the transformer during this time interval. The equation is solved for $V_{PRI}(t)$ and the result is given in (10). This process is repeated for all of the subintervals. Finding an equation for the primary voltage allows the current through the resonant inductance to be calculated; this equation will be used later in the derivation to ultimately determine the resonant inductance required in order to achieve ZVS.

$$V_{PRI}(t) = \frac{L_M \cdot ((L_R \cdot n \cdot (V_{OUT} + 2 \cdot V_{RD})) + (L_0 \cdot V_S))}{L_0 \cdot (L_M + L_R) + (L_M \cdot L_R \cdot n^2)} \quad (10)$$

when $t_0 \leq t < t_1$.

B. Operation During $t = t_1$ to t_2 (active to passive transition time)

At the beginning of this period switch S_A turns off and switch S_D remains on. This period is the active to passive zero voltage transition period and the duration of this period is given in Equation 11 [14].

$$t_{1,2} = \frac{2 \cdot C_R \cdot V_S}{n \cdot I_O} \quad (11)$$

At the end of this period the voltage at point A in Figure 1 is clamped to one forward diode drop below ground as the diode in anti-parallel with switch S_B is now forward biased. The changes in current over this time period are derived by integrating over the transition time $t_{1,2}$.

$$\Delta I_{L_R}(t_1, t_2) = \int_{t_1}^{t_2} \frac{V_{L_R}(t_1, t_2)}{L_R} .dt \quad (12)$$

$$\Delta I_{L_M}(t_1, t_2) = \int_{t_1}^{t_2} \frac{V_{L_M}(t_1, t_2)}{L_M} .dt \quad (13)$$

$$\Delta I_{L_0}(t_1, t_2) = \int_{t_1}^{t_2} \frac{V_{L_0}(t_1, t_2)}{L_0} .dt \quad (14)$$

The relationship between the changes in current remains the same as (6) in the first interval as the reflected output current is still flowing through the primary current path. However, the three key voltages change during this period. It has been identified that the primary current during this interval is much larger than that required to charge and discharge the parasitic capacitances [13]. Thus, the change in each voltage is almost linear during this period. The voltage across the resonant inductance at the beginning of the time period, t_1 , and at the end of the time period, t_2 , can therefore be defined by analyzing the voltages around the closed loop at each of these respective time periods. The voltage across the inductances at the beginning and end of this time period are defined in (15) to (18).

$$V_{L_R}(t_1) = V_S - V_{PRI}(t_0, t_1) \quad (15)$$

$$V_{L_R}(t_2) = -V_{PRI}(t_2, t_3) - V_{MD} \quad (16)$$

$$V_{L_M}(t_1) = V_{PRI}(t_0, t_1) \quad (17)$$

$$V_{L_M}(t_2) = V_{PRI}(t_2, t_3) \quad (18)$$

The voltage across the output filter inductor is the same as the previous interval. The integrations of (12) to (14) are performed using the voltages defined in (15) to (18).

$$\begin{aligned} V_{PRI}(t) = & \{L_M \cdot (-L_R \cdot n \cdot t_{1,2} \cdot (V_{OUT} + 2 \cdot V_{RD})) \\ & - L_M \cdot L_0 \cdot (-t_{1,2} \cdot V_S + t \cdot (V_{MD} + V_S))\} / \\ & ((L_0 \cdot (L_M + L_R) + L_M \cdot L_R \cdot n^2) \cdot t_{1,2}) \end{aligned} \quad (19)$$

when $t_1 \leq t < t_2$.

C. Operation During $t = t_2$ to t_3

This period lasts for $t_{DT} - t_{1,2}$. Current freewheels around the loop through the intrinsic diode of the MOSFET switch S_B .

$$V_{L_0}(t_2, t_3) = n.V_{PRI} - 2.V_{RD} - V_{OUT} \quad (20)$$

$$V_{L_R}(t_2, t_3) = -V_{PRI}(t_2, t_3) - V_{MD} \quad (21)$$

$$V_{L_M}(t_2, t_3) = V_{PRI}(t_2, t_3) \quad (22)$$

$$V_{PRI}(t) = \frac{L_M \cdot ((-L_0 \cdot V_{MD}) + (L_R \cdot n \cdot (V_{OUT} + 2 \cdot V_{RD})))}{L_0 \cdot (L_M + L_R) + (L_M \cdot L_R \cdot n^2)} \quad (23)$$

when $t_2 \leq t < t_3$.

D. Operation During $t = t_3$ to t_4

At the beginning of this period, switch S_B turns on with zero voltage across it. The current freewheeling around the primary is shared between the intrinsic diode and MOSFET channel of S_B . This freewheeling period is equal to the time when duty is not applied to the primary winding of the transformer minus two dead-time periods. This is defined in (24).

$$t_{3,4} = \left((1 - D) \cdot \frac{T}{2} \right) - 2 \cdot t_{DT} \quad (24)$$

During the freewheeling period there is a positive voltage across L_M and a negative voltage across L_R . The dot end of the primary winding is positive and the dot end of the secondary is also positive.

$$V_{L_0}(t_3, t_4) = n.V_{PRI} - 2.V_{RD} - V_{OUT} \quad (25)$$

$$V_{L_R}(t_3, t_4) = -V_{PRI}(t_3, t_4) \quad (26)$$

$$V_{L_M}(t_3, t_4) = V_{PRI}(t_3, t_4) \quad (27)$$

$$V_{PRI}(t) = \frac{L_R \cdot L_M \cdot n \cdot (V_{OUT} + 2 \cdot V_{RD})}{L_0 \cdot (L_M + L_R) + (L_M \cdot L_R \cdot n^2)} \quad (28)$$

when $t_3 \leq t < t_4$.

E. Operation During $t = t_4$ to t_5 (passive to active transition time)

At the end of the freewheeling period S_D is turned off marking the beginning of this period. The voltage at point B in Figure 1 will rise from zero to $V_S + V_{MD}$. The magnetizing inductance will oppose this change by generating a positive voltage at the bottom of the transformer primary windings with respect to the dot at the top. Thus, the voltage across the secondary will start to fall.

However, when the secondary voltage reaches below the conduction voltage of the bridge diodes, all four diodes in the bridge will attempt to turn off, cutting off the output inductance from the primary current path. The output inductance will attempt to maintain the current and will impress a back EMF in such a way that all secondary bridge diodes will become forward biased at the same time.

At this point the voltage across the secondary is clamped to near zero as all of the bridge diodes are conducting and consequently the voltage across the primary is also forced to near zero. Hence, the full $V_S + V_{MD}$ voltage will be impressed across the resonant inductance. The energy stored in the resonant inductance is the sole inductance that attempts to maintain the flow of current in the primary path as the output inductor is now effectively disconnected from the primary. Therefore this transition period is fundamentally different to the previous transition period.

The capacitor across switch S_D is charged and the capacitor across switch S_C is discharged in a time $t_{4,5}$. This period is the passive to active zero voltage transition period and is equal to one quarter of the resonant period as calculated in (29) [13]. The resonant tank is formed from the resonant inductance, L_R , and a combination of the parasitic non-linear drain-source capacitances of the MOSFETs combined with any transformer winding capacitance, C_R .

$$t_{4,5} = \frac{\pi}{2} \cdot \sqrt{L_R \cdot \frac{C_R}{8}} \quad (29)$$

At the end of this period, the voltage at point B in Figure 1 is clamped at one forward diode drop above the supply voltage as the diode in anti-parallel with switch S_C is now forward biased. Current through the primary can now begin increasing in the opposite direction to the previous cycle.

The voltages during this period can be described as one quarter of a sine wave whilst the resonant capacitors charge and discharge. However, the transition time periods are short in comparison to the other intervals within the switching period. Therefore, a straight line transition can be used to describe the changes in current during this interval as the difference between using a sinusoid and straight line is minor, as will be shown in both the simulated and experimental results. The changes in current over this time period are defined as:

$$\Delta I_{L_R}(t_4, t_5) = \int_0^{t_{4,5}} \frac{V_{L_R}(t_4, t_5)}{L_R} \cdot dt \quad (30)$$

$$\Delta I_{L_M}(t_4, t_5) = \int_0^{t_{4,5}} \frac{V_{L_M}(t_4, t_5)}{L_M} \cdot dt \quad (31)$$

$$\Delta I_{L_0}(t_4, t_5) = \int_0^{t_{4,5}} \frac{V_{L_0}(t_4, t_5)}{L_0} \cdot dt \quad (32)$$

Where the voltages at the beginning and end of this time period are:

$$V_{L_R}(t_4) = -V_{PRI}(t_3, t_4). \quad (33)$$

$$V_{L_R}(t_5) = -V_S - V_{MD}. \quad (34)$$

$$V_{L_M}(t_4) = V_{PRI}(t_3, t_4). \quad (35)$$

$$V_{L_M}(t_5) \approx 0. \quad (36)$$

By the end of this period the voltage across the secondary winding of the transformer will collapse to near zero as all of the rectifying diodes become forward biased clamping the secondary winding to near zero volts.

$$V_{L_0}(t_4) = n \cdot V_{PRI}(t_3, t_4) - 2 \cdot V_{RD} - V_{OUT}. \quad (37)$$

$$V_{L_0}(t_5) = 0 - 2 \cdot V_{RD} - V_{OUT}. \quad (38)$$

Thus, the voltage across the primary side of the transformer will also collapse to near zero by the end of this period. This transition can be described by a straight line equation using the value of $V_{PRI}(t)$ at the end of the last period.

$$\begin{aligned} V_{PRI}(t) &= \frac{0 - V_{PRI}(t_3, t_4)}{t_{4,5}} \cdot t + V_{PRI}(t_3, t_4) \\ &= \frac{-L_M \cdot L_R \cdot n \cdot (V_{OUT} + 2 \cdot V_{RD}) \cdot (t - t_{4,5})}{(L_0 \cdot (L_M + L_R) + (L_M \cdot L_R \cdot n^2)) \cdot t_{4,5}} \end{aligned} \quad (39)$$

when $t_4 \leq t < t_5$.

F. Operation During $t = t_5$ to t_6

During this period switch S_B is on and current is flowing through the diode in anti-parallel with switch S_C . The voltage at point B in Figure 1 remains clamped at one forward diode drop above the supply voltage during this period which lasts for $t_{DT} - t_{4,5}$. The current in the primary continues to ramp towards zero in the opposite direction to the previous time periods.

It is imperative that the switch S_C is turned on at the end of this period before the primary current reaches zero. If switch S_C is not turned on, and the primary current reaches zero, the voltage at point B will fall very rapidly

from one diode drop above the supply voltage to zero. ZVS would be lost as the voltage across switch S_C would no longer be near zero.

$$V_{L_0}(t_5, t_6) = 0 - 2.V_{RD} - V_{OUT} \quad (40)$$

$$V_{L_R}(t_5, t_6) = -V_S - V_{MD} \quad (41)$$

$$V_{L_M}(t_5, t_6) \approx 0 \quad (42)$$

Given (42), the voltage across the primary of the transformer remains at near zero for this period.

$$V_{PRI}(t) \approx 0 \quad (43)$$

when $t_5 \leq t < t_6$.

G. Operation During $t = t_6$ to t_7

At the end of the last period, t_6 , the dead-time will have expired. The switch S_C is turned on with zero voltage across it momentarily before the primary current reaches zero. This event marks the beginning of this period in which both switches S_C and S_B are on. The supply voltage V_S is impressed across L_R and L_M . However, the voltage across $V_{PRI}(t)$, and thus $L_M(t)$, is still clamped to zero by the bridge rectifying diodes. The current through the resonant inductance and primary current path is therefore forced to ramp in the opposite direction through zero and towards a negative value.

During this period switch S_C and S_B are on and power should be being delivered to the load. However, no power is delivered to the load as the voltage across the secondary winding is clamped to near zero. This effect accounts for the reduced duty period on the secondary side of the transformer and is referred to as the lost duty period, ΔD . This lost duty increases in size as the resonant inductance size increases. Therefore, the resonant inductance should be kept to the minimum value required in order to achieve ZVS across the desired load range and to keep this duty cycle loss period to a minimum.

The end of this period occurs when the secondary current becomes equal to the output inductor current. At this point the output inductor current can be fully supplied from the transformer secondary current. Only at this point can some of the rectifying diodes in the bridge turn off; the diodes change state and become a bridge rectifier again.

This period lasts for $((D - D_{EFF}) \cdot \frac{T}{2})$ and ends when the primary current reaches the negative of the starting current, $-I_P$.

$$V_{L_0}(t_6, t_7) = 0 - 2.V_{RD} - V_{OUT} \quad (44)$$

$$V_{L_R}(t_6, t_7) = -V_S \quad (45)$$

$$V_{L_M}(t_6, t_7) = 0 \quad (46)$$

$$V_{PRI}(t_6, t_7) = 0 \quad (47)$$

The key currents at the end of this time period, t_7 , are equal in magnitude to the starting currents:

$$I_{L_R}(t_7) = -I_P \quad (48)$$

$$I_{L_M}(t_7) = -I_{MAG} \quad (49)$$

$$I_{L_0}(t_7) = I_S \quad (50)$$

All of the equations necessary for calculating the required resonant inductance in (2) have now been defined. The full equation for calculating the resonant inductance is given in (51).

$$L_R = \frac{-(V_S + V_{MD}) \cdot (t_{DT} - t_{4,5})}{0 - I_{L_R}(t_5)} \quad (\text{for } t_{DT} > t_{4,5}) \quad (51)$$

Where $t_{4,5}$ is defined in (29). The required key current, $I_{L_R}(t_5)$, can now be calculated given the change in currents over each of the time periods.

$$I_{L_R}(t_5) = I_P + \sum_{n=0}^4 \Delta I_{L_R}(t_n, t_{n+1}) \quad (52)$$

Where the initial primary current is given in (53).

$$I_P = I_{MAG} + n \cdot I_S \quad (53)$$

The full equations for each of the resonant inductor current time periods are presented in the Appendix.

IV. EQUATION VERIFICATION

As was the case in the work by Sabate et al. [13], an iterative algorithm to calculate the required resonant inductance is proposed. The initial value for the resonant inductance should be set equal to the value of the transformer leakage inductance. The change in current during each sub-interval can be evaluated in order to find $I_{L_R}(t_5)$ after the calculation of D , D_{EFF} and $t_{4,5}$ using this initial resonant inductance. The derived equations for calculating D and D_{EFF} are provided in the Appendix.

TABLE I
PSFB CONVERTER SPECIFICATION

Parameter	Value	Parameter	Value
V_S	40Vdc	t_{DEAD}	166.67ns
V_O	5.0Vdc	V_{MD}	0.842V
$I_{O(MIN)}$	2.5A	V_{RD}	0.842V
C_O	940μF	L_M	117μH
L_O	2μH	C_{OSS}	200pF
n	2/6	R_{MIN}	1.2Ω
F_S	200kHz	R_{MAX}	2.0Ω
C_R	200pF	ΔI_{L_0}	2.78A

Following this, all of the values required to calculate the resonant inductance are known. The new value for the resonant inductance is found using (51) and this process is repeated until a suitably accurate value of resonant inductance is found which does not differ between two consecutive calculation runs.

The derived equations are verified through the use of a simulated and experimental PSFB design. Table I provides the specification for the PSFB design. For this example, a steady inductance accurate to eight decimal places is reached after fifteen iterations. The required inductance is calculated at the minimum load at which ZVS should be achieved, 2.0Ω. The required resonant inductance is calculated as:

$$L_R = 8.19\mu H \quad D = 0.5661 \quad D_{EFF} = 0.5543$$

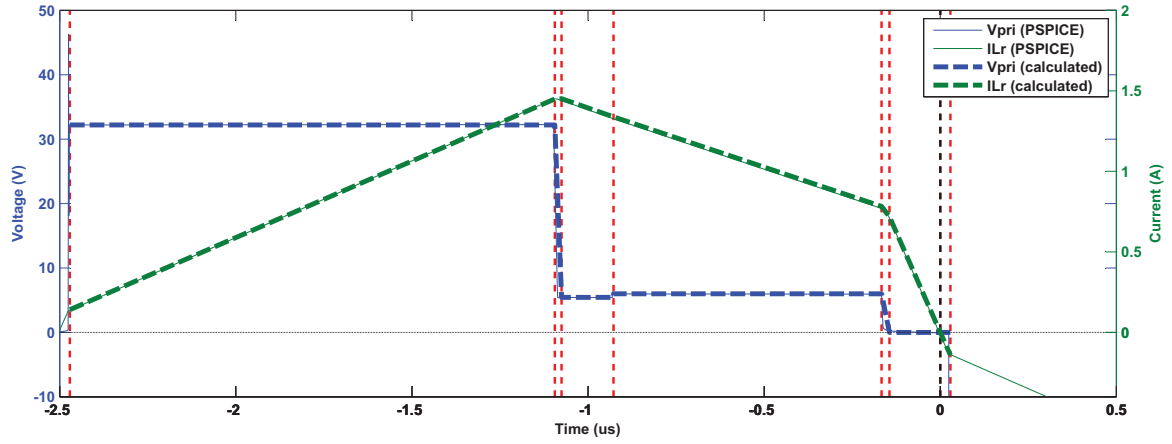
A. Simulation Verification

First, the equations describing the operation of the converter are verified against a PSPICE simulated PSFB converter using the example PSFB design. The simulation has a maximum step size of 1ns and is run for 5ms by which time the converter is operating in steady state.

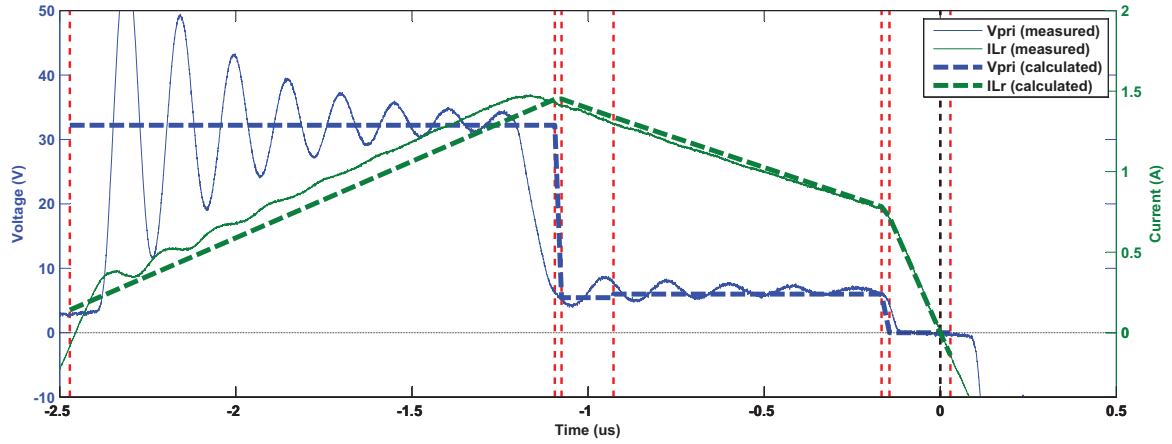
Figure 3a compares the voltage and currents from the PSPICE simulation to those calculated using the equations derived in Section III. There is an excellent correlation between the two sets of results. The calculated values (dashed lines) are identical to the PSPICE simulated values (solid lines).

Tables II and III compare the calculated and simulated values for the key voltages and currents respectively during each time interval. The key voltages given in Table II are taken at the mid point of the time interval. The change in the key currents over each time interval are given in Table III.

There is excellent correlation between the two sets of results and the percentage difference is small, less than 2%, for all of the time intervals. The straight line equation discussed earlier to describe the key voltages during



(a) Comparison of derived time interval equation to PSPICE simulated waveforms for an example PSFB converter



(b) Comparison of derived time interval equation to oscilloscope captured waveform from hardware PSFB converter.

Fig. 3. Verifying derived time interval equations using simulated and hardware comparisons.

the transition periods $t_{1,2}$ and $t_{4,5}$ produces accurate results for the calculated change in current. The difference between the calculated and simulated results during these transition intervals is always less than 10mA . These results indicate that the derived time interval equations are an accurate representation of the PSPICE converter simulation. This is further confirmed in the next section through a hardware verification.

B. Hardware Verification

A PSFB converter is constructed in hardware using a transformer with a turns ratio of $n = 2/6$. This transformer is accurately characterized in order to determine the leakage inductance. An OMICRON Labs Bode 100 vector network analyzer is used to perform a frequency sweep to measure the impedance of the transformer. An additional inductance of $7.5\mu\text{H}$ is combined in series with the measured leakage inductance of $0.64\mu\text{H}$. The total measured resonant inductance is $8.14\mu\text{H}$ at 200kHz . The D and D_{EFF} equations are recalculated using $L_R = 8.14\mu\text{H}$.

TABLE II
PERCENTAGE DIFFERENCE BETWEEN THE PSFB CALCULATED AND SIMULATED VOLTAGE EQUATIONS FOR EACH TIME INTERVAL.

	$V_{L_R}(t)$	$V_{L_M}(t)$	$V_{L_0}(t)$
$t_0 \rightarrow t_1$	-0.058%	0.021%	-0.090%
$t_1 \rightarrow t_2$	$f(t)$	$f(t)$	$f(t)$
$t_2 \rightarrow t_3$	-0.269%	-0.256%	-0.268%
$t_3 \rightarrow t_4$	0.022%	0.057%	0.024%
$t_4 \rightarrow t_5$	$f(t)$	$f(t)$	$f(t)$
$t_5 \rightarrow t_6$	-0.038%	n/a	1.172%
$t_6 \rightarrow t_7$	0.418%	n/a	1.702%

TABLE III
PSFB CALCULATED AND SIMULATED CHANGE IN CURRENT FOR EACH TIME PERIOD. ALL VALUES IN AMPERES.

	$\Delta I_{L_R}(t)$		$\Delta I_{L_M}(t)$		$\Delta I_{L_0}(t)$	
	Calc	Sim	Calc	Sim	Calc	Sim
t_0, t_1	1.309	1.314	0.379	0.380	2.789	2.797
t_1, t_2	0.002	0.001	0.003	0.002	-0.004	-0.003
t_2, t_3	-0.113	-0.119	0.007	0.007	-0.359	-0.379
t_3, t_4	-0.556	-0.555	0.039	0.039	-1.784	-1.783
t_4, t_5	-0.064	-0.061	0.001	0.000	-0.064	-0.071
t_5, t_6	-0.718	-0.719	0.000	0.000	-0.482	-0.476
t_6, t_7	-0.141	-0.126	0.000	0.000	-0.096	-0.085

$$D = 0.5674 \quad D_{EFF} = 0.5548$$

A TMS320F28035 microcontroller from Texas Instruments is used to provide the PWM driving signals for the MOSFETs of the full bridge converter. A microcontroller is chosen as this provides a convenient method of adjusting the phase shift and dead-time on-the-fly without the need to change component values. It also allows the system to be run with a specified fixed duty, or phase shift, for direct comparison to the simulated example. This also eliminates the issue of flux imbalance in the transformer core as the net volt-second product applied to the core is zero. A controller could be implemented, however, the solution must address the issue of flux imbalance within the core and prevent saturation which would result in considerable core losses. This can be implemented using the same microcontroller through means of peak current mode control [26].

Figure 3b overlays the raw oscilloscope data with the calculated results from the derived time interval equations.

The results taken from the hardware implementation show an excellent correlation with the calculated results. The dashed vertical line at $t = 0$ indicates that the resonant inductor primary current crosses the zero axis precisely as the switch is turned on. Ringing on the primary and secondary windings is commonplace with PSFB converters and severely increases the overall losses of the converter. This will be shown in Section IV-D. It is possible to clamp this ringing using clamping diodes, however, this is at the expense of increased losses at light loads [27].

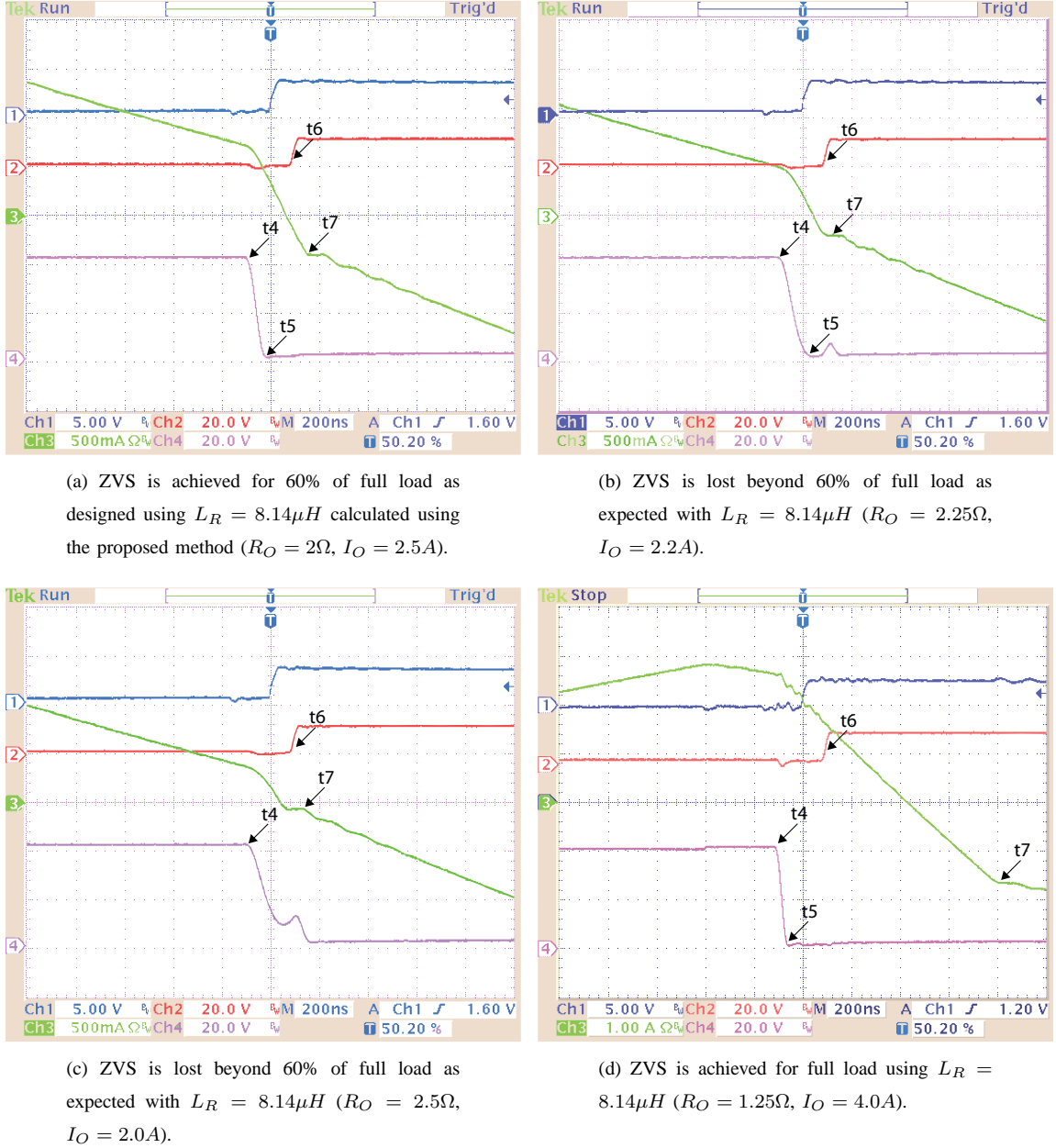


Fig. 4. Ch1: Switch PWM. Ch2: Switch gate-source voltage. Ch3: Resonant inductor current, $I_{L_R}(t)$. Ch4: Switch drain-to-source voltage.

Figure 4a shows a zoomed oscilloscope plot of the voltage across the parasitic drain-to-source capacitor of the

MOSFET (Ch4) collapsing to zero before the MOSFET is turned on with a 2.0Ω load (60% of full load) precisely as predicted by the equations. The hardware verification uses $L_R = 8.14\mu H$ as the resonant inductance, calculated using the proposed design method, and $166.67ns$ of dead-time. The MOSFET turns on with zero voltage across it and thus minimal turn-on losses. Furthermore, the primary current through the resonant inductor crosses zero immediately after the switch is turned on; thus minimizing the lost duty period.

In Figure 4b the load resistance is increased to 2.25Ω . This is beyond the design point used in the proposed equations for achieving ZVS. Therefore, according to the equations, ZVS should be lost at this point. In Figure 4b the drain-source voltage initially collapses to zero and the switch could be turned on with zero voltage across it, however, the dead-time lasts until t_6 . The current through the resonant inductor collapses to zero and thus the voltage across the switch begins to increase. However, at this point the dead-time expires and the switch is turned on with some voltage across it. Therefore this is not zero voltage switching and has been accurately predicted by the equations. Similarly in Figure 4c the load resistance is increased further to 2.5Ω and the current through the resonant inductor collapses the zero sooner. The switch is turned on with voltage across it and thus losses.

In Figure 4d the load resistance has been decreased to 1.25Ω , increasing the current through the resonant inductor. ZVS is achieved comfortably at this load level. However, the duty cycle loss period, ΔD extends until t_7 as the current through the resonant inductance must ramp to the reflected output current. This further confirms the importance of selecting the minimum resonant inductance required to achieve ZVS.

C. Comparison to Other Models

Previous work [13] has suggested that the size of the required resonant inductance is solely based on the energy stored in the parasitic capacitances at the time when the passive-to-active switches must be turned on. In (54) the equation for calculating the resonant inductance under this condition is presented [13].

$$L_R = \frac{4.C_R.L_0^2.N_P^2.V_{IN}^2}{N_S^2.(\Delta I_{L_0}.L_0 + 2.I_O.L_0 - T.V_{OUT} + D.T.V_{OUT})^2} \quad (54)$$

When the design parameters given in Table I are entered into (54), the result is calculated as $L_R = 2.14\mu H$. This is considerably less than the $L_R = 8.14\mu H$ calculated using the proposed design equations. It has already been shown in Figure 4b that ZVS is lost as the operation of the converter passes the design point of $I_O = 2.5A$, and the output current decreases, with $L_R = 8.14\mu H$. Therefore, it is clear that ZVS would not be achieved at this design point with a smaller resonant inductance of $L_R = 2.14\mu H$. This smaller value of resonant inductance is because previous analyses did not take in to consideration the length of dead-time in the calculation of the resonant inductance. Furthermore, the more complete model proposed in this paper includes the contribution from the magnetizing current which would assist in ZVS.

D. Optimum Efficiency

The efficiency plot of the PSFB converter is provided in Figure 5. This Figure proves that the design point used to calculate the resonant inductance, when $I_o = 2.5A$, results in the point of maximum efficiency. This is because

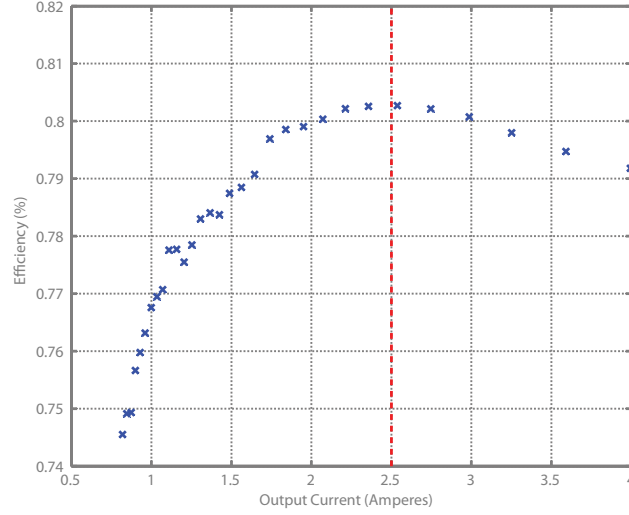


Fig. 5. Measured efficiency of the hardware converter showing the design point $I_O = 2.5A$.

the duty cycle loss period, ΔD , has been reduced to a minimum at this point whilst achieving ZVS as shown in the previous Figure 4a. The overall efficiency can be increased by addressing the issue of ringing across the transformer windings and the reverse recovery loss of the rectifying diodes. These factors contribute a significant proportion of losses in PSFB converters [28]. This proof of concept design confirms the validity of the equations, however, it also suffers from a significant loss overhead which reduces the overall efficiency.

E. Parameter Variations

The equation for calculating the required resonant inductance has now been fully defined and verified. Therefore, it is now possible to examine how this required resonant inductance varies with the other design parameters. In Section I it was suggested that transformers with a low magnetizing inductance and thus high magnetizing current could achieve ZVS for a wider load range as this magnetizing current assists in the resonant transition [14], [17].

In Figure 6a, the required resonant inductance is calculated for varying values of magnetizing inductance. All of the remaining design parameters remain the same as in Table I. The relationship between the two inductances confirms this statement. It can be seen that the required resonant inductor approaches an asymptote as the magnetizing inductance increases and thus the magnetizing current becomes small in comparison to the resonant inductor current.

Furthermore, in Section II it was suggested that as the required dead-time increases so too would the required resonant inductance as the current through the resonant inductor must not cross the zero axis before the dead-time expires and the next switch is turned on. Figure 6b shows the relationship between the fixed dead-time and the required resonant inductance. The figure supports this statement. Thus, it is advantageous for the dead-time to be as small as is required by the MOSFET switches and gate drive circuitry.

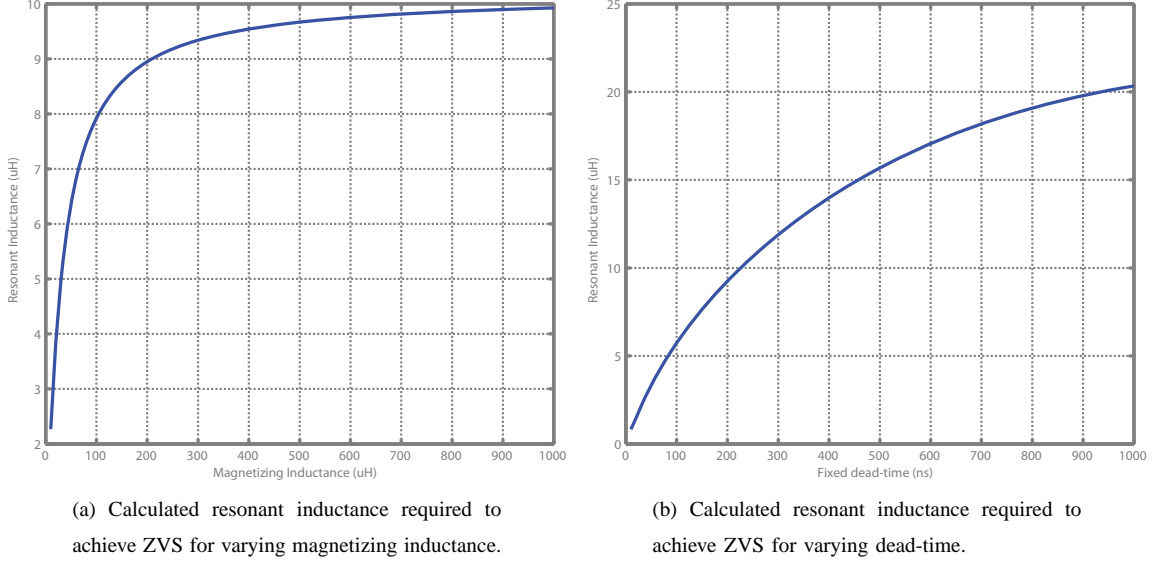


Fig. 6. Single design parameter variation affecting required resonant inductance. Other design parameters remained fixed according to specification.

V. CONCLUSION

The work presented in this paper builds on previous analyzes of the PSFB converter [13], [12], [29] to include the effects of the magnetizing inductance and dead-time into the operation of the converter. This paper presents an entirely new and unique set of design equations that allow the resonant inductance to be analytically calculated in order to achieve ZVS across a wide load range given a fixed magnetizing inductance and dead-time. The method used in this paper has been verified through simulations and finally a hardware implementation.

The hardware verification indicated that ZVS is achieved from full load to minimum load. The analysis presented in this paper has shown that ZVS can be achieved for a minimum load if the resonant inductor current reaches zero immediately after the end of the dead-time. Furthermore, the relationship between magnetizing inductance, dead-time and required resonant inductance has been investigated.

The equation given for L_R enables the resonant inductance to be selected in order for ZVS to be achieved. The calculated resonant inductance minimizes the duty cycle loss period, ΔD , by ensuring that the resonant current is zero immediately following the turn on of the final switch in the sequence. This condition enables maximum load regulation over the widest possible ZVS range.

APPENDIX A EQUATIONS

$$L_D = L_0 (L_M + L_R) + L_M \cdot L_R \cdot n^2 \quad (55)$$

$$\Delta I_{L_R}(t_0, t_1) = \frac{D_{EFF}.T.(L_0.V_S + L_M.n.(-V_O - 2.V_{RD} + n.V_S))}{2.L_D} \quad (56)$$

$$\Delta I_{L_R}(t_1, t_2) = \frac{-t_{1,2}.(L_0.(V_{MD} - V_S) + L_M.n.(n.V_{MD} + 2.V_O + 4.V_{RD} - n.V_S))}{2.L_D} \quad (57)$$

$$\Delta I_{L_R}(t_2, t_3) = \frac{-(t_D - t_{1,2}).(L_0.V_{MD} + L_M.n.(n.V_{MD} + V_O + 2.V_{RD}))}{L_D} \quad (58)$$

$$\Delta I_{L_R}(t_3, t_4) = \frac{L_M.n.((D-1).T + 4.t_D).(V_O + 2.V_{RD})}{2.L_D} \quad (59)$$

$$\Delta I_{L_R}(t_4, t_5) = \frac{-t_{4,5}.(L_0.(L_M + L_R).(V_{MD} + V_S) + L_M.L_R.n.(V_O + 2.V_{RD} + n.(V_{MD} + V_S)))}{2.L_D} \quad (60)$$

$$t_E = -D_{EFF}.T + D.T + 2.t_D \quad (61)$$

$$t_F = D_{EFF}.T - 2.t_D + t_{4,5} \quad (62)$$

$$V_A = V_{MD} + V_S \quad (63)$$

$$V_B = V_O + 2.V_{RD} \quad (64)$$

$$D_A = -2 + D_{EFF} \quad (65)$$

$$D_B = -2 + 2.D_{EFF} \quad (66)$$

$$D_C = -1 + 2.D_{EFF} \quad (67)$$

$$L_T = L_M + L_R \quad (68)$$

$$\begin{aligned} I_S &= \frac{1}{4.L_0.L_D.T}. \\ &\left[4.I_O.L_0.L_D.T + L_M.L_R.n^2.(t_E^2 - 2.t_E.t_{4,5} + 2.t_{4,5}^2).V_B + L_0.(L_R.T^2.V_B + L_M.(T^2.V_B + \right. \\ &\left. n(-4.t_D^2.V_{MD} + D_A.D_{EFF}.T^2.V_S + 2.t_{1,2}^2.V_A - D_B.T.(2.t_D.V_{MD} - t_{1,2}.V_A)))) \right] \end{aligned} \quad (69)$$

$$I_{MAG} = \frac{1}{4.L_D} \cdot [-L_R.n.((1 + D_{EFF} - D).T - 2.t_D + t_{4,5}).V_B + L_0.(2.t_D.V_{MD} - D_{EFF}.T.V_S - t_{1,2}.V_A)] \quad (70)$$

$$(71)$$

$$D_{EFF} = \frac{1}{L_M.n.T.(L_R.n.V_B + L_0.V_S) \cdot [L_M.L_R.n^2.(D.T + 2.t_D - t_{4,5}).V_B + L_0.(L_R.T.V_B + L_M.(T.V_B + n.(2.t_D.V_{MD} - t_{1,2}.V_A)))]} \quad (72)$$

$$(73)$$

$$D = \frac{1}{2.L_M.L_R^2.n^3.T^2.V_B \cdot [T.(-L_R.n.(L_0.L_T.T - 2.L_M.L_R.n^2.t_F). (V_B + L_0.L_D.T.V_S) \pm \sqrt{R_D})]} \quad (74)$$

$$R_D = T^2 \cdot [-16.I_O.L_0.L_M.L_R^3.n^4.L_D.T.V_B - 4.L_M^2.L_R^4.n^6.t_{4,5}^2.V_B^2 + L_0^4.L_T^2.T^2.V_S^2 - 2.L_0^3.L_R.L_T.n.T^2.V_S.(L_T.V_B - L_M.n.V_S) - 4.L_0.L_M^2.L_R^3.n^5.V_B. ((-4D_{EFF}.T.t_D - 4.t_D^2 + T.t_{4,5} + D_C.T.t_{1,2} + 2.t_{1,2}^2).V_{MD} + ((-1 + D_{EFF}).D_{EFF}.T^2 + D_C.T.t_{1,2} + 2.t_{1,2}^2).V_S) + L_0^2.L_R^2.n^2.T.(L_T.V_B.(8.L_M.n.t_D.V_{MD} - 4.L_M.n.t_{4,5}.V_{MD} + L_M.T.V_O + L_R.T.V_O + 2.L_T.T.V_{RD}) - 2.L_M.L_T.n.T.V_B.V_S + L_M^2.n^2.T.V_S^2)] \quad (75)$$

$$\begin{aligned}
L_0 = & -\frac{1}{8.I_{O(MIN)}.(L_M + L_R).T}. \\
& (4.I_{O(MIN)}.L_M.L_R.n^2.T + 4.L_M.n.T.t_D.V_{MD} - \\
& 4.D_{EFF}.L_M.n.T.t_D.V_{MD} - \\
& 4.L_M.n.t_D^2.V_{MD} - 2.L_M.n.T.t_{1,2}.V_{MD} + \\
& 2.D_{EFF}.L_M.n.T.t_{1,2}.V_{MD} + \\
& 2.L_M.n.t_{1,2}^2.V_{MD} + L_M.T^2.V_O + \\
& L_R.T^2.V_O + 2.L_M.T^2.V_{RD} + \\
& 2.L_R.T^2.V_{RD} - 2.D_{EFF}.L_M.n.T^2.V_S + \\
& D_{EFF}^2.L_M.n.T^2.V_S - 2.L_M.n.T.t_{1,2}.V_S + \\
& 2.D_{EFF}.L_M.n.T.t_{1,2}.V_S + \\
& 2.L_M.n.t_{1,2}^2.V_S \pm \sqrt{R_L})
\end{aligned}$$

$$\begin{aligned}
R_L = & (-16.I_{O(MIN)}.L_M.L_R.L_T.n^2.T. \\
& (t_E^2 - 2.t_E.t_{4,5} + 2.t_{4,5}^2).V_B + \\
& (4.I_O.L_M.L_R.n^2.T + L_R.T^2.V_B +)^2 \\
& L_M.(T^2.V_B + n(-4.t_D^2.V_{MD} + \\
& D_A.D_{EFF}.T^2.V_S + 2.t_{1,2}^2.V_A - \\
& D_B.T.(2.t_D.V_{MD} - t_{1,2}.V_A)))^2)
\end{aligned} \tag{76}$$

$$I_{O(MIN)} = I_O/5 \tag{77}$$

REFERENCES

- [1] L. Mweene, C. Wright, and M. Schlecht, "A 1 kw 500 khz front-end converter for a distributed power supply system," *Power Electronics, IEEE Transactions on*, vol. 6, no. 3, pp. 398–407, Jul. 1991.
- [2] K.-H. Liu and F. Lee, "Zero-voltage switching technique in dc/dc converters," *Power Electronics, IEEE Transactions on*, vol. 5, no. 3, pp. 293–304, Jul. 1990.
- [3] M. Jovanovic, W. Tabisz, and F. Lee, "Zero-voltage-switching technique in high-frequency off-line converters," in *Applied Power Electronics Conference and Exposition, 1988. APEC '88. Conference Proceedings 1988., Third Annual IEEE*, Feb 1988, pp. 23–32.
- [4] Y. Jang, M. Jovanovic, and Y.-M. Chang, "A new zvs-pwm full-bridge converter," *Power Electronics, IEEE Transactions on*, vol. 18, no. 5, pp. 1122–1129, sept. 2003.
- [5] Y. Jang and M. Jovanovic, "A new family of full-bridge zvs converters," *Power Electronics, IEEE Transactions on*, vol. 19, no. 3, pp. 701–708, may 2004.

- [6] J. Dudrik and N.-D. Trip, "Soft-switching ps-pwm dc-dc converter for full-load range applications," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2807–2814, aug. 2010.
- [7] A. Elasser, M. Schutten, V. Vlatkovic, D. Torrey, and M. Kheraluwala, "Switching losses of igbts under zero-voltage and zero-current switching," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, vol. 1, jun 1996, pp. 600–607 vol.1.
- [8] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *Power Electronics, IEEE Transactions on*, vol. 3, no. 2, pp. 174–182, Apr 1988.
- [9] D. Maksimovic and S. Cuk, "Constant-frequency control of quasi-resonant converters," *Power Electronics, IEEE Transactions on*, vol. 6, no. 1, pp. 141–150, Jan 1991.
- [10] K. D. T. K. M. H. Fisher, R. A.; Ngo, "A 500 khz, 250 w dc-dc converter with multiple outputs controlled by phase-shifted pwm and magnetic amplifiers," *High frequency power conversion*, vol. 3rd international conference, pp. 100–110, 1988.
- [11] Y. Jiang, Z. Chen, and J. Pan, "Zero-voltage switching phase shift full-bridge step-up converter with integrated magnetic structure," *Power Electronics, IET*, vol. 3, no. 5, pp. 732–739, september 2010.
- [12] V. Vlatkovic, J. Sabate, R. Ridley, F. Lee, and B. Cho, "Small-signal analysis of the phase-shifted pwm converter," *Power Electronics, IEEE Transactions on*, vol. 7, no. 1, pp. 128–135, Jan 1992.
- [13] J. Sabate, V. Vlatkovic, R. Ridley, F. Lee, and B. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched pwm converter," in *Applied Power Electronics Conference and Exposition, Fifth Annual*, mar 1990, pp. 275–284.
- [14] K. Papastergiou and D. Macpherson, "An airborne radar power supply with contactless transfer of energy part ii: Converter design," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 5, pp. 2885–2893, Oct. 2007.
- [15] G.-B. Koo, G.-W. Moon, and M.-J. Youn, "Analysis and design of phase shift full bridge converter with series-connected two transformers," *Power Electronics, IEEE Transactions on*, vol. 19, no. 2, pp. 411–419, march 2004.
- [16] R. Watson and F. Lee, "Analysis, design, and experimental results of a 1-kw zvs-fb-pwm converter employing magamp secondary-side control," *Industrial Electronics, IEEE Transactions on*, vol. 45, no. 5, pp. 806–814, oct 1998.
- [17] M. Kheraluwala, R. Gascoigne, D. Divan, and E. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *Industry Applications, IEEE Transactions on*, vol. 28, no. 6, pp. 1294–1301, nov/dec 1992.
- [18] W. Chen, F. Lee, M. Jovanovic, and J. Sabate, "A comparative study of a class of full bridge zero-voltage-switched pwm converters," no. 0, mar 1995, pp. 893–899 vol.2.
- [19] J. Zhang, X. Xie, X. Wu, and Z. Qian, "Comparison study of phase-shifted full bridge zvs converters," in *Power Electronics Specialist Conference*, vol. 1, June 2004, pp. 533–539 Vol.1.
- [20] X. Wu, J. Zhang, X. Xie, and Z. Qian, "Analysis and optimal design considerations for an improved full bridge zvs dc-dc converter with high efficiency," *Power Electronics, IEEE Transactions on*, vol. 21, no. 5, pp. 1225–1234, sept. 2006.
- [21] Y. Jang and M. Jovanovic, "A new pwm zvs full-bridge converter," *Power Electronics, IEEE Transactions on*, vol. 22, no. 3, pp. 987–994, may 2007.
- [22] B.-H. Kwon, J.-H. Kim, and G.-Y. Jeong, "Full-bridge soft switching pwm converter with saturable inductors at the secondary side," *Electric Power Applications, IEE Proceedings -*, vol. 146, no. 1, pp. 117–122, jan 1999.
- [23] R. L. Steigerwald, "Full-bridge lossless switching converter," US Patent 4864479, 1989.
- [24] I.-H. Cho, K.-M. Cho, J.-W. Kim, and G.-W. Moon, "A new phase-shifted full-bridge converter with maximum duty operation for server power system," *Power Electronics, IEEE Transactions on*, vol. 26, no. 12, pp. 3491–3500, dec. 2011.
- [25] C.-S. Yun, B.-C. Kim, K.-H. Kim, Y.-C. Lim, and P. Freere, "Reducing the high frequency transformer losses in an fb zvt pwm converter," *Electric Power Applications, IEE Proceedings -*, vol. 149, no. 2, pp. 161–164, mar 2002.
- [26] M. Hallworth and S. Shirsavar, "Microcontroller based peak current mode control using digital slope compensation," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, p. 1, 2011.
- [27] W. Chen, X. Ruan, Q. Chen, and J. Ge, "Zero-voltage-switching pwm full-bridge converter employing auxiliary transformer to reset the clamping diode current," *Power Electronics, IEEE Transactions on*, vol. 25, no. 5, pp. 1149–1162, may 2010.
- [28] M. Ilic and D. Maksimovic, "Phase-shifted full bridge dc-dc converter with energy recovery clamp and reduced circulating current," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 25 2007-march 1 2007, pp. 969–975.
- [29] M. Schutten and D. Torrey, "Improved small-signal analysis for the phase-shifted pwm power converter," *Power Electronics, IEEE Transactions on*, vol. 18, no. 2, pp. 659–669, mar 2003.

M. Hallworth (M'11) received the B.Eng. (Hons.) degree in Electronic Engineering from the University of Reading, Reading, U.K., in 2009. Currently working towards a Ph.D. at the same University. His main research topic is in the field of high efficiency contactless power conversion. Other related interests include power electronics, microcontrollers and embedded systems design.

B. A. Potter (M'06) received the M.Eng. (Hons.) degree in Engineering Science from the University of Oxford, Oxford, U.K., and the Ph.D degree from the University of Reading in 2001 and 2007 respectively. He is currently a Lecturer at the University of Reading where his main research interests include renewable energy, smart power grids and efficient power conversion.

S. A. Shirsavar received the B.Eng. (Hons.) degree in Electronic Engineering and the Ph.D. degree from the University of Reading, Reading, U.K., in 1992 and 1998, respectively. After a period of work in the industry designing embedded controller hardware, switch-mode power supplies, and high-performance three-phase inverters, he returned to the University of Reading as a Lecturer, where he has been teaching courses at all levels. His main research interests are in power electronics and renewable energy resources, in particular high-efficiency grid-connected inverters for use with solar panels.